Mitigating Soft Errors And Process Variations

This volume presents the proceedings of the First Euro-China Conference on Intelligent Data Analysis and Applications (ECC 2014), which was hosted by Shenzhen Graduate School of Harbin Institute of Technology and was held in Shenzhen City on June 13-15, 2014. ECC 2014 was technically co-sponsored by Shenzhen Municipal People's Government, IEEE Signal Processing Society, Machine Intelligence Research Labs, VSB-Technical University of Ostrava (Czech Republic), National Kaohsiung University of Applied Sciences (Taiwan), and Secure E-commerce Transactions (Shenzhen) Engineering Laboratory of Shenzhen Institute of Standards and Technology.

This book evaluates the influence of process variations (e.g. work-function fluctuations) and radiation-induced soft errors in a set of logic cells using FinFET technology, considering the 7nm technological node as a case study. Moreover, for accurate soft error estimation, the authors adopt a radiation event generator tool (MUSCA SEP3), which deals both with layout features and electrical properties of devices. The authors also explore four circuit-level techniques (e.g. transistor reordering, decoupling cells, Schmitt Trigger, and sleep transistor) as alternatives to attenuate the unwanted effects on FinFET logic cells. This book also evaluates the mitigation tendency when different levels of process variation, transistor sizing, and radiation particle characteristics are applied in the design. An overall comparison of all methods addressed by this work is provided allowing to trace a trade-off between the reliability gains and the design penalties of each approach regarding the area, performance, power consumption, single event transient (SET) pulse width, and SET cross-section.

This book constitutes the proceedings of the 34th International Conference on Architecture of Computing Systems, ARCS 2021, held virtually in July 2021. The 12 full papers in this volume were carefully reviewed and selected from 24 submissions. 2 workshop papers (VEFRE) are also included. ARCS has always been a conference attracting leading-edge research outcomes in Computer Architecture and Operating Systems, including a wide spectrum of topics ranging from fully integrated, self-powered embedded systems up to high-performance computing systems. It also provides a platform covering newly emerging and cross-cutting topics, such as autonomous and ubiquitous systems, reconfigurable computing and acceleration, neural networks and artificial intelligence. The selected papers cover a variety of topics from the ARCS core domains, including heterogeneous computing, memory optimizations, and organic computing.

This book provides a detailed treatment of radiation effects in electronic devices, including effects at the material, device, and circuit levels. The emphasis is on transient effects caused by single ionizing particles (single-event effects and soft errors) and effects produced by the cumulative energy deposited by the radiation (total ionizing dose effects). Bipolar (Si and SiGe), metalOCooxideOCosemiconductor (MOS), and compound semiconductor technologies are discussed. In addition to considering the specific issues associated with high-performance devices and technologies, the book includes the background material necessary for understanding radiation effects at a more general level. Contents: Single Event Effects in Avionics and on the Ground (E Normand); Soft Errors in Commercial Integrated Circuits (R C Baumann); System Level Single Event Upset Mitigation Strategies (W F Heidergott); Space Radiation Effects in Optocouplers (R A Reed et al.); The Effects of Space Radiation Exposure on Power MOSFETs: A Review (K Shenai et al.); Total Dose Effects in Linear Bipolar Integrated Circuits (H J Barnaby); Hardness Assurance for Commercial Microelectronics (R L Pease); Switching Oxide Traps (T R Oldham); Online and Realtime Dosimetry Using Optically Stimulated Luminescence (L Dusseau & J Gasiot); and other articles. Readership: Practitioners, researchers, managers and graduate students in electrical and electronic engineering, semiconductor science and technology, and microelectronics."

This volume contains revised and extended research articles written by prominent researchers. Topics covered include electrical engineering, circuits, artificial intelligence, data mining, imaging engineering, bioinformatics, internet computing, software engineering, and industrial applications. The book offers tremendous state-of-the-art advances in electrical engineering and also serves as an excellent reference work for researchers and graduate students working with/on electrical engineering.

Energetic particle (alpha particle, cosmic neutron, etc.) induced single event data upset or soft error has emerged as a key reliability concern in SRAMs in sub-100 nanometre technologies. Low operating voltage, small node capacitance, high packing density, and lack of error masking mechanisms are primarily responsible for the soft error susceptibility of SRAMs. In addition, since SRAM occupies the majority of die area in system-on-chips (SoCs) and microprocessors, different leakage reduction techniques, such as, supply voltage reduction, gated grounding, etc., are applied to SRAMs in order to limit the overall chip leakage. These leakage reduction techniques exponentially increase the soft error rate in SRAMs. The soft error rate is further accentuated by process variations, which are prominent in scaled-down technologies. In this research, we address these concerns and propose techniques to characterize and mitigate soft errors in nanoscale SRAMs. We develop a comprehensive analytical model of the critical charge, which is a key to assessing the soft error susceptibility of SRAMs. The model is based on the dynamic behaviour of the cell and a simple decoupling technique for the non-linearly coupled storage nodes. The model describes the critical charge in terms of NMOS and PMOS transistor parameters, cell supply voltage, and noise current parameters. Consequently, it enables characterizing the spread of critical charge due to process induced variations in these parameters and to manufacturing defects, such as, resistive contacts or vias. In addition, the model can estimate the improvement in critical charge when MIM capacitors are added to the cell in order to improve the soft error robustness. The model is validated by SPICE simulations (90nm CMOS) and radiation test.

This book constitutes the proceedings of the 5th International Workshop on Design, Modeling, and Evaluation of Cyber Physical Systems, CyPhy 2015, held as part of ESWeek 2015, in Amsterdam, The Netherlands, in October 2015. The 10 papers presented in this volume were carefully reviewed and selected from 13 submissions. They broadly interpret, from a diverse set of disciplines, the modeling, simulation, and evaluation of cyber-physical systems.

Soft Error Mitigation Techniques for Future Chip Multiprocessors
Modeling and Mitigation of Soft Errors in Nanoscale SRAMs
Circuits and Statistical Design for Yield
Process-Aware SRAM Design and Test
Computer Engineering and Technology
24th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2016, Tallinn, Estonia, September 26-28, 2016, Revised Selected Papers
Soft Error Reliability of VLSI Circuits
Euro-Par 2018: Parallel Processing Workshops
A Cross Layer Perspective
Dependability in Electronic Systems
VLSI Design and Test for Systems Dependability
Cyber Physical Systems. Design, Modeling, and Evaluation

The monograph will be dedicated to SRAM (memory) design and test issues in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.

The sustained drive to downsize the transistors has reached a point where device sensitivity against transient faults due to neutron and alpha particle strikes a.k.a soft errors has moved to the forefront of concerns for next-generation designs. Following Moore's law, the exponential growth in the number of transistors per chip has brought tremendous progress in the performance and functionality of processors. However, incorporating billions of transistors into a chip makes it more likely to encounter a soft soft errors. Moreover, aggressive voltage scaling and process variations make the processors even more vulnerable to soft errors. Also, the number of cores on chip is growing exponentially fueling the multicore revolution. With increased core counts and larger memory arrays, the total failure-in-time (FIT) per chip (or package) increases. Our studies concluded that the shrinking technology required to match the power and performance demands for servers and future exa- and tera-scale systems impacts the FIT budget. New soft error mitigation techniques that allow meeting the failure rate target are important to keep harnessing the benefits of Moore's law. Traditionally, reliability research has focused on providing circuit, microarchitecture and architectural solutions, which include device hardening, redundant execution, lock-step, error correcting codes, modular redundancy etc. In general, all these techniques are very effective in handling soft errors but expensive in terms of performance, power, and area overheads. Traditional solutions fail to scale in providing the required degree of reliability with increasing failure rates while maintaining low area, power and performance cost. Moreover, this family of solutions has hit the point of diminishing return, and simply achieving 2X improvement in the soft error rate may be impractical. Instead of relying on some kind of redundancy, a new direction that is growing in interest by the research community is detecting the actual particle strike rather than its consequence. The proposed idea consists of deploying a set of detectors on silicon that would be in charge of perceiving the particle strikes that can potentially create a soft error. Upon detection, a hardware or software mechanism would trigger the appropriate recovery action. This work proposes a lightweight and scalable soft error mitigation solution. As a part of our soft error mitigation technique, we show how to use acoustic wave detectors for detecting and locating particle strikes. We use them to protect both the logic and the memory arrays, acting as unified error detection mechanism. We architect an error containment mechanism and a unique recovery mechanism based on checkpointing that works with acoustic wave detectors to effectively recover from soft errors. Our results show that the proposed mechanism protects the whole processor (logic, flip-flop, latches and memory arrays) incurring minimum overheads.

This book covers the practical application of dependable electronic systems in real industry, such as space, train control and automotive control systems, and network servers/routers. The impact from intermittent errors caused by environmental radiation (neutrons and alpha particles) and EMI (Electro-Magnetic Interference) are introduced together with their most advanced countermeasures. Power Integration is included as one of the most important bases of dependability in electronic systems. Fundamental technical background is provided, along with practical design examples. Readers will obtain an overall picture of dependability from failure causes to countermeasures for their relevant systems or products, and therefore, will be able to select the best choice for maximum dependability.

This book constitutes the refereed proceedings of the Third International Conference on Wireless, Mobile Networks and Applications, WiMoA 2011, and the First International Conference on Computer Science, Engineering and Applications, ICCSEA 2011, held in Dubai, United Arab Emirates, in May 2011. The book is organized as a collection of papers from WiMoA 2011 and ICCSEA 2011. The 8 revised full papers presented in the WiMoA 2011 part were carefully reviewed and selected from 63 submissions. The 20 revised full papers presented in the ICCSEA 2011 part were carefully reviewed and selected from 110 submissions.

Analysis and Design of Resilient VLSI CircuitsMitigating Soft Errors and Process VariationsSpringer Science & Business Media

Architecture Design for Soft Errors provides a comprehensive description of the architectural techniques to tackle the soft error problem. It covers the new methodologies for quantitative analysis of soft errors as well as novel, cost-effective architectural techniques to mitigate them. To provide readers with a better grasp of the broader problem definition and solution space, this book also delves into the physics of soft errors and reviews current circuit and software mitigation techniques. There are a number of different ways this book can be read or used in a course: as a complete course on architecture design for soft errors covering the entire book; a short course on architecture design for soft errors; and as a reference book on classical fault-tolerant machines. This book is recommended for practitioners in semi-conductor industry, researchers and developers in computer architecture, advanced graduate seminar courses on soft errors, and (iv) as a reference book for undergraduate courses in computer architecture. Helps readers build-in fault tolerance to the billions of microchips produced each year, all of which are subject to soft errors Shows readers how to quantify their soft error reliability Provides state-of-the-art techniques to protect against soft errors

This book describes novel software concepts to increase reliability under user-defined constraints. The authors' approach bridges, for the first time, the reliability gap between hardware and software. Readers will learn how to achieve increased soft error resilience on unreliable hardware, while exploiting the inherent error masking characteristics and error (stemming from soft errors, aging, and process variations) mitigations potential at different software layers.

Architecture of Computing Systems
Euro-Par 2018 International Workshops, Turin, Italy, August 27-28, 2018, Revised Selected Papers
Proceedings of TCCE 2020
Proceedings of International Conference on Trends in Computational and Cognitive Engineering
FPGA Architecture
International Conferences, WiMoA 2011 and ICCSEA 2011, Dubai, United Arab Emirates, May 25-27, 2011. Proceedings
IAENG Transactions on Electrical Engineering, Volume 1
VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability
Special issue of the International Multiconference of Engineers and Computer Scientists 2012. Volume 1
Architecture Design for Soft Errors
VLSI
Clocking in Modern VLSI Systems

This book discusses the new roles that the VLSI (very-large-scale integration of semiconductor circuits) is taking for the safe, secure, and dependable design and operation of electronic systems. The book consists of three parts. Part I, as a general introduction to this vital topic, describes how electronic systems are designed and tested with particular emphasis on dependability engineering, where the simultaneous assessment of the detrimental outcome of failures and cost of their containment is made. This section also describes the related research project "Dependable VLSI Systems," in which the editor and authors of the book were involved for 8 years. Part II addresses various threats to the dependability of VLSIs as key systems components, including time-dependent degradations, variations in device characteristics, ionizing radiation, electromagnetic interference, design errors, and tampering, with discussion of technologies to counter those threats. Part III elaborates on the design and test technologies for dependability in such applications as control of robots and vehicles, data processing, and storage in a cloud environment and heterogeneous wireless telecommunications. This book is intended to be used as a reference for engineers who work on the design and testing of VLSI systems with particular attention to dependability. It can be used as a textbook in graduate courses as well. Readers interested in dependable systems from social and industrial–economic perspectives will also benefit from the discussions in this book.

This book constitutes the refereed proceedings of the 19th CCF Conference on Computer Engineering and Technology, NCCET 2015, held in Hefei, China, in October 2015. The 18 papers presented were carefully reviewed and selected from 158 submissions. They are organized in topical sections on processor architecture; application specific processors; computer application and software optimization; technology on the horizon.

This book provides comprehensive coverage of the dependability challenges in today's advanced computing systems. It is an in-depth discussion of all the technological and design-level techniques that may be used to overcome these issues and analyzes various dependability-assessment methods. The impact of individual application scenarios on the definition of challenges and solutions is considered so that the designer can clearly assess the problems and adjust the solution based on the specifications in question. The book is composed of three sections, beginning with an introduction to current dependability challenges arising in complex computing systems implemented with nanoscale technologies, and of the effect of the application scenario. The second section details all the fault-tolerance techniques that are applicable in the manufacture of reliable advanced computing devices. Different levels, from technology-level fault avoidance to the use of error correcting codes and system-level checkpointing are introduced and explained as applicable to the different application scenario requirements. Finally the third section proposes a roadmap of future trends in and perspectives on the dependability and manufacturability of advanced computing systems from the special point of view of industrial stakeholders. Dependable Multicore Architectures at Nanoscale showcases the original ideas and concepts introduced into the field of nanoscale manufacturing and systems reliability over nearly four years of work within COST Action IC1103 MEDIAN, a think-tank with participants from 27 countries. Academic researchers and graduate students working in multi-core computer systems and their manufacture will find this book of interest as will industrial design and manufacturing engineers working in VLSI companies.

This book provides the reader with knowledge on a wide varietyof radiation fields and their effects on the electronic devices andsystems. The author covers faults and failures in ULSI devicesinduced by a wide variety of radiation fields, including electrons,alpha-rays, muons, gamma rays, neutrons and heavy ions. Readerswill learn how to make numerical models from physical insights, todetermine the kind of mathematical approaches that should beimplemented to analyze radiation effects. A wide variety ofprediction, detection, characterization and mitigation techniquesagainst soft-errors are reviewed and discussed. The author showshow to model sophisticated radiation effects in condensed matter inorder to quantify and control them, and explains how electronicsystems including servers and routers are shut down due toenvironmental radiation. Provides an understanding of how electronic systems are shutdown due to environmental radiation by constructing physical modelsand numerical algorithms Covers both terrestrial and avionic-level conditions Logically presented with each chapter explaining the backgroundphysics to the topic followed by various modelling techniques, andchapter summary Written by a widely-recognized authority in soft-errors inelectronic devices Code samples available for download from the CompanionWebsite This book is targeted at researchers and graduate students innuclear and space radiation, semiconductor physics and electrondevices, as well as other areas of applied physics modelling.Researchers and students interested in how a variety of physicalphenomena can be modelled and numerically treated will also findthis book to present helpful methods.

This book contains extended and revised versions of the best papers presented at the 24th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2016, held in Tallinn, Estonia, in September 2016. The 11 papers included in the book were carefully reviewed and selected from the 36 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the latest scientific and industrial results and developments as well as future trends in the field of System-on-Chip (SoC) Design.

This book provides a comprehensive presentation of the most advanced research results and technological developments enabling understanding, qualifying and mitigating the soft errors effect in advanced electronics, including the fundamental physical mechanisms of radiation induced soft errors, the various steps that lead to a system failure, the modelling and simulation of soft error at various levels (including physical, electrical, netlist, event driven, RTL, and system level modelling and simulation), hardware fault injection, accelerated radiation testing and natural environment testing, soft error oriented test structures, process-level, device-level, cell-level, circuit-level, architectural-level, software level and system level soft error mitigation techniques. The book contains a comprehensive presentation of most recent advances on understanding, qualifying and mitigating the soft error effect in advanced electronic systems, presented by academia and industry experts in reliability, fault tolerance, EDA, processor, SoC and system design, and in particular, experts from industries that have faced the soft error impact in terms of product reliability and related business issues and were in the forefront of the countermeasures taken by these companies at multiple levels in order to mitigate the soft error effects at a cost acceptable for commercial products. In a fast moving field, where the impact on ground level electronics is very recent and its severity is steadily increasing at each new process node, impacting one after another various industry sectors (as an example, the Automotive Electronics Council comes to publish qualification requirements on soft errors), research and technology developments and industrial practices have evolve very fast, outdating the most recent books edited at 2004.

The two volume set LNCS 7439 and 7440 comprises the proceedings of the 12th International Conference on Algorithms and Architectures for Parallel Processing, ICA3PP 2012, as well as some workshop papers of the CDCN 2012 workshop which was held in conjunction with this conference. The 40 regular paper and 26 short papers included in these proceedings were carefully reviewed and selected from 156 submissions. The CDCN workshop attracted a total of 19 original submissions, 8 of which are included in part II of these proceedings. The papers cover many dimensions of parallel algorithms and architectures, encompassing fundamental theoretical approaches, practical experimental results, and commercial components and systems.

Terrestrial Neutron-Induced Soft Errors in Advanced Memory Devices
Advances in Wireless, Mobile Networks and Applications
Mitigating Process Variability and Soft Errors at Circuit-Level for FinFETs
12th International Conference, ICA3PP 2012, Fukuoka, Japan, September 4-7, 2012, Proceedings
Soft Error Reliability Using Virtual Platforms
Special Issue of the International MultiConference of Engineers and Computer Scientists 2012
34th International Conference, ARCS 2021, Virtual Event, June 7-8, 2021 : Proceedings
CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies
Iaeng Transactions on Electrical Engineering
Dependable Multicore Architectures at Nanoscale
Mitigating Soft Errors and Process Variations
5th International Workshop, CyPhy 2015, Amsterdam, The Netherlands, October 8, 2015, Proceedings

This book is intended for readers who are interested in the design of robust and reliable electronic digital systems. The authors cover emerging trends in design of today's reliable electronic systems which are applicable to safety-critical applications, such as automotive or healthcare electronic systems. The emphasis is on modeling approaches and algorithms for analysis and mitigation of soft errors in nano-scale CMOS digital circuits, using techniques that are the cornerstone of Computer Aided Design (CAD) of reliable VLSI circuits. The authors introduce software tools for analysis and mitigation of soft errors in electronic systems, which can be integrated easily with design flows. In addition to discussing soft error aware analysis techniques for combinational logic, the authors also describe new soft error mitigation strategies targeting commercial digital circuits. Coverage includes novel Soft Error Rate (SER) analysis techniques such as process variation aware SER estimation and GPU accelerated SER analysis techniques, in addition to SER reduction methods such as gate sizing and logic restructuring based SER techniques.

. . . ???????????????????????????????? ????????????? ????????????,????? ???? ??????????? ???????????????????? ???. THUCYDIDIS HISTORIAE IV:108 C. Hude ed. , Teubner, Lipsiae MCMXIII ???????????,????? ??,? ????????????????? ??????????????????? ?????? ?????? ?????? ??? ????????? ??? ?' ?????????? ??' ?????????? ? ??????? ??? ????????????? ???????. ???????????????????:108 ???????????? ?????????????????????? ?. ?????????????. ????????????,????? It being the fashion of men, what they wish to be true to admit even

upon an ungrounded hope, and what they wish not, with a magistral kind of arguing to reject. Thucydides (the Peloponnesian War Part I), IV:108 Thomas Hobbes Trans. , Sir W. Molesworth ed. In The English Works of Thomas Hobbes of Malmesbury, Vol. VIII I have been introduced to clock design very early in my professional career when I was tapped right out of school to design and implement the clock generation and distribution of the Alpha 21364 microprocessor. Traditionally, Alpha processors - hibited highly innovative clocking systems, always worthy of ISSCC/JSSC publi- tions and for a while Alpha processors were leading the industry in terms of clock performance. I had huge shoes to ?ll. Obviously, I was overwhelmed, confused and highly con?dent that I would drag the entire project down.

This book constitutes revised selected papers from of the workshops held at 24th International Conference on Parallel and Distributed Computing, Euro-Par 2018, which took place in Turin, Italy, in August 2018. The 64 full papers presented in this volume were carefully reviewed and selected from 109 submissions. Euro-Par is an annual, international conference in Europe, covering all aspects of parallel and distributed processing. These range from theory to practice, from small to the largest parallel and distributed systems and infrastructures, from fundamental computational problems to full-edged applications, from architecture, compiler, language and interface design and implementation to tools, support infrastructures, and application performance aspects.

This book describes the benefits and drawbacks inherent in the use of virtual platforms (VPs) to perform fast and early soft error assessment of multicore systems. The authors show that VPs provide engineers with appropriate means to investigate new and more efficient fault injection and mitigation techniques. Coverage also includes the use of machine learning techniques (e.g., linear regression) to speed-up the soft error evaluation process by pinpointing parameters (e.g., architectural) with the most substantial impact on the software stack dependability. This book provides valuable information and insight through more than 3 million individual scenarios and 2 million simulation-hours. Further, this book explores machine learning techniques usage to navigate large fault injection datasets.

Variability is one of the most challenging obstacles for IC design in the nanometer regime. In nanometer technologies, SRAM show an increased sensitivity to process variations due to low-voltage operation requirements, which are aggravated by the strong demand for lower power consumption and cost, while achieving higher performance and density. With the drastic increase in memory densities, lower supply voltages, and higher variations, statistical simulation methodologies become imperative to estimate memory yield and optimize performance and power. This book is an invaluable reference on robust SRAM circuits and statistical design methodologies for researchers and practicing engineers in the field of memory design. It combines state of the art circuit techniques and statistical methodologies to optimize SRAM performance and yield in nanometer technologies. Provides comprehensive review of state-of-the-art, variation-tolerant SRAM circuit techniques; Discusses Impact of device related process variations and how they affect circuit and system performance, from a design point of view; Helps designers optimize memory yield, with practical statistical design methodologies and yield estimation techniques.

Recently the world celebrated the 60th anniversary of the invention of the first transistor. The first integrated circuit (IC) was built a decade later, with the first microprocessor designed in the early 1970s. Today, ICs are a part of nearly every aspect of our daily lives. They help us live longer and more comfortably, and do more, faster. All this is possible because of the relentless search for new materials, circuit designs, and ideas happening on a daily basis at industrial and academic institutions around the globe. Showcasing the latest advances in very-large-scale integrated (VLSI) circuits, VLSI: Circuits for Emerging Applications provides a balanced view of industrial and academic developments beyond silicon and complementary metal-oxide-semiconductor (CMOS) technology. From quantum-dot cellular automata (QCA) to chips for cochlear implants, this must-have resource: Investigates the trend of combining multiple cores in a single chip to boost performance of the overall system Describes a novel approach to enable physically unclonable functions (PUFs) using intrinsic features of a VLSI chip Examines the VLSI implementations of major symmetric and asymmetric key cryptographic algorithms, hash functions, and digital signatures Discusses nonvolatile memories such as resistive random-access memory (Re-RAM), magneto-resistive RAM (MRAM), and floating-body RAM (FB-RAM) Explores organic transistors, soft errors, photonics, nanoelectromechanical (NEM) relays, reversible computation, bioinformatics, asynchronous logic, and more VLSI: Circuits for Emerging Applications presents cutting-edge research, design architectures, materials, and uses for VLSI circuits, offering valuable insight into the current state of the art of micro- and nanoelectronics.

Ionizing Radiation Effects in Electronics: From Memories to Imagers delivers comprehensive coverage of the effects of ionizing radiation on state-of-the-art semiconductor devices. The book also offers valuable insight into modern radiation-hardening techniques. The text begins by providing important background information on radiation effects, their underlying mechanisms, and the use of Monte Carlo techniques to simulate radiation transport and the effects of radiation on electronics. The book then: Explains the effects of radiation on digital commercial devices, including microprocessors and volatile and nonvolatile memories—static random-access memories (SRAMs), dynamic random-access memories (DRAMs), and Flash memories Examines issues like soft errors, total dose, and displacement damage, together with hardening-by-design solutions for digital circuits, field-programmable gate arrays (FPGAs), and mixed-analog circuits Explores the effects of radiation on fiber optics and imager devices such as complementary metal-oxide-semiconductor (CMOS) sensors and charge-coupled devices (CCDs) Featuring real-world examples, case studies, extensive references, and contributions from leading experts in industry and academia, Ionizing Radiation Effects in Electronics: From Memories to Imagers is suitable both for newcomers who want to become familiar with radiation effects and for radiation experts who are looking for more advanced material or to make effective use of beam time.

Soft Errors in Modern Electronic Systems
Terrestrial Radiation Effects in ULSI Devices and Electronic Systems
From Memories to Imagers
Survey and Challenges
Analysis and Design of Resilient VLSI Circuits
19th CCF Conference, NCCET 2015, Hefei, China, October 18-20, 2015, Revised Selected Papers
Circuits for Emerging Applications
Analysis and Mitigation Techniques

Soft Error Analysis and Mitigation in Circuits Involving C-elements
Nanometer Variation-Tolerant SRAM
Proceeding of the First Euro-China Conference on Intelligent Data Analysis and Applications, June 13-15, 2014, Shenzhen, China

Terrestrial neutron-induced soft errors in semiconductor memory devices are currently a major concern in reliability issues. Understanding the mechanism and quantifying soft-error rates are primarily crucial for the design and quality assurance of semiconductor memory devices.This book covers the relevant up-to-date topics in terrestrial neutron-induced soft errors, and aims to provide succinct knowledge on neutron-induced soft errors to the readers by presenting several valuable and unique features.

FPGA Architecture: Survey and Challenges reviews the historical development of programmable logic devices, the fundamental programming technologies that the programmability is built on, and then describes the basic understandings gleaned from research on architectures. It is an invaluable reference for engineers and computer scientists. It is also an excellent primer for senior or graduate-level students in electrical engineering or computer science.

This monograph is motivated by the challenges faced in designing reliable VLSI systems in modern VLSI processes. The reliable operation of integrated circuits (ICs) has become increasingly dif?cult to achieve in the deep submicron (DSM) era. With continuouslydecreasing device feature sizes, combinedwith lower supply voltages and higher operating frequencies, the noise immunity of VLSI circuits is decreasing alarmingly. Thus, VLSI circuits are becoming more vulnerable to noise effects such as crosstalk, power supply variations, and radiation-inducedsoft errors. Among these noise sources, soft errors(or error caused by radiation particle strikes) have become an increasingly troublesome issue for memory arrays as well as c- binational logic circuits. Also, in the DSM era, process variations are increasing at a signi?cant rate, making it more dif?cult to design reliable VLSI circuits. Hence, it is important to ef?ciently design robust VLSI circuits that are resilient to radiation particle strikes and process variations. The work presented in this research mo- graph presents several analysis and design techniques with the goal of realizing VLSI circuits, which are radiation and process variation tolerant.

Ionizing Radiation Effects in Electronics
Intelligent Data analysis and its Applications, Volume II
Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices
Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances
Algorithms and Architectures for Parallel Processing
Reliable Software for Unreliable Hardware
Soft-error Mitigation at the Architecture-level Using Berger Codes for Error Detection
Terrestrial Neutron-induced Soft Errors in Advanced Memory Devices
Efficient Techniques for Modeling and Mitigation of Soft Errors in Nanometer-scale Static CMOS Logic Circuits
Early Evaluation of Multicore Systems