Delay Models For Cmos Circuits

The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published Low-Power Electronics Design, Low-Power CMOS Circuits: Technology, Logic Design, and CAD Tools addresses the design of low-power circuitry in deep submicron technologies. It provides a focused reference for specialists involved in designing low-power circuitry, from transistors to logic gates. The book is organized into three broad sections for convenient access. The first examines the history of low-power electronics along with a look at emerging and possible future technologies. It also considers other technologies, such as nanotechnologies and optical chips, that may be useful in designing integrated circuits. The second part explains the techniques used to reduce power consumption at low levels. These include clock gating, leakage reduction, interconnecting and communication on chips, and adiabatic circuits. The final section discusses various CAD tools for designing low-power circuits. This section includes three chapters that demonstrate the tools and low-power design issues at three major companies that produce logic synthesizers. Providing detailed examinations contributed by leading experts, Low-Power CMOS Circuits:

Technology, Logic Design, and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits. It is a must-read for anyone designing modern computers or embedded systems. Welcome to the proceedings of PATMOS 2005, the 15th in a series of international workshops.PATMOS2005wasorganizedbyIMECwithtechnicalco-sponsorshipfrom the IEEE Circuits and Systems Society. Over the years, PATMOS has evolved into an important European event, where - searchers from both industry and academia discuss and investigate the emerging ch- lenges in future and contemporary applications, design methodologies, and tools - quired for the developmentof upcominggenerationsof integrated circuits and systems. The technical program of PATMOS 2005 contained state-of-the-art technical contri- tions, three invited talks, a special session on hearing-aid design, and an embedded - torial. The technical program focused on timing, performance and power consumption, as well as architectural aspects with particular emphasis on modeling, design, char- terization, analysis and optimization in the nanometer era. The Technical Program Committee, with the assistance of additional expert revi- ers, selected the 74 papers to be presented at PATMOS. The papers were divided into 11 technical sessions and 3 poster sessions.

As is always the case with the PATMOS workshops, the review process was anonymous, full papers were required, and several reviews were carried out per paper. Beyond the presentations of the papers, the PATMOS technical program was - riched by a series of speeches offered by world class experts, on important emerging research issues of industrial relevance. Prof. Jan Rabaey, Berkeley, USA, gave a talk on "Traveling the Wild Frontier of Ulta Low-Power Design", Dr. Sung Bae Park, S- sung, gave a presentation on "DVL (Deep Low Voltage): Circuits and Devices", Prof. ThefourinvitedtalksaddresstheEuropeanresearch activitiesinthewo- shop?elds,theevolvingneedsfo rminimalpowerconsumptioninthe areaof wirelessa ndchipcardapplicationsanddesignmethodologieso fveryhighly- tegratedmultimediaprocessors. The workshopisaresultofthejointworkofalargenumber ofindividuals, whocannotallbementionedhere. Inparticular,wewouldliketoacknowledge theoutst andingworkofthereviewers,whodidacompetentjo binatimely manner. Wealsohavetothankthememb ersofthelocalorganizingcommittee fortheire?ortin enablingtheconferencetorunsmoothly. Finally,wegratefully acknowledgethesupportofall organizationsandinstitutionssponsoringthe conference.

This book presents MOSFET-based current mode logic (CML) topologies, which increase the speed, and lower the transistor count, supply voltage

and power consumption. The improved topologies modify the conventional PDN, load, and the current source sections of the basic CML gates. Electronic system implementation involves embedding digital and analog circuits on a single die shifting towards mixed-mode circuit design. The high-resolution, low-power and low-voltage analog circuits are combined with high-frequency complex digital circuits, and the conventional static CMOS logic generates large current spikes during the switching (also referred to as digital switching noise), which degrade the resolution of the sensitive analog circuits via supply line and substrate coupling. This problem is exacerbated further with scaling down of CMOS technology due to higher integration levels and operating frequencies. In the literature, several methods are described to reduce the propagation of the digital switching noise. However, in high-resolution applications, these methods are not sufficient. The conventional CMOS static logic is no longer an effective solution, and therefore an alternative with reduced current spikes or that draws a constant supply current must be selected. The current mode logic (CML) topology, with its unique property of requiring constant supply current, is a promising alternative to the conventional CMOS static logic.

This book provides a comprehensive review of the state-of-the-art in the development of new

and innovative materials, and of advanced modeling and characterization methods for nanoscale CMOS devices. Leading global industry bodies including the International Technology Roadmap for Semiconductors (ITRS) have created a forecast of performance improvements that will be delivered in the foreseeable future – in the form of a roadmap that will lead to a substantial enlargement in the number of materials, technologies and device architectures used in CMOS devices. This book addresses the field of materials development, which has been the subject of a major research drive aimed at finding new ways to enhance the performance of semiconductor technologies. It covers three areas that will each have a dramatic impact on the development of future CMOS devices: global and local strained and alternative materials for high speed channels on bulk substrate and insulator; very low access resistance; and various high dielectric constant gate stacks for power scaling. The book also provides information on the most appropriate modeling and simulation methods for electrical properties of advanced MOSFETs, including ballistic transport, gate leakage, atomistic simulation, and compact models for single and multi-gate devices, nanowire and carbon-based FETs. Finally, the book presents an in-depth investigation of the main nanocharacterization techniques that can be used for an accurate

determination of transport parameters, interface defects, channel strain as well as RF properties, including capacitance-conductance, improved split C-V, magnetoresistance, charge pumping, low frequency noise, and Raman spectroscopy. Timing, memory, power dissipation, testing, and testability are all crucial elements of VLSI circuit design. In this volume culled from the popular VLSI Handbook, experts from around the world provide in-depth discussions on these and related topics. Stacked gate, embedded, and flash memory all receive detailed treatment, including their power consumption and recent developments in low-power memories. Reflecting the rapid development and importance of systems-on-a-chip (SOCs), an entire chapter is devoted to application-specific integrated circuits (ASICs). Design-related topics include microprocessor architectures, layout methods, design verification, testability concepts, and various CAD tools. .

Analog Design Issues in Digital VLSI Circuits and Systems brings together in one place important contributions and up-to-date research results in this fast moving area. Analog Design Issues in Digital VLSI Circuits and Systems serves as an excellent reference, providing insight into some of the most challenging research issues in the field.

17th International Workshop, PATMOS 2007, Gothenburg, Sweden, September 3-5, 2007,

Proceedings
Model and Design of Improved Current Mode Logic Gates
Low Power Interconnect Design
Improvement of a Propagation Delay Model for CMOS Digital Logic Circuits
Proceedings of the XVII Conference on Design of Circuits and Integrated Systems, Santander, Spain, November 19-22, 2002
IFIP TC10 / WG10.5 Eleventh International Conference on Very Large Scale Integration of Systems-on-Chip (VLSI-SOC'01) December 3-5, 2001, Montpellier, France
Integrated Circuit Design: Power and Timing Modeling, Optimization and Simulation
Portland Hilton, Portland, OR, May 8-11, 1989
Through Silicon Vias
1989 IEEE International Symposium on Circuits and Systems
CMOS Digital Integrated Circuits

Este libro contiene las presentaciones de la XVII Conferencia de Diseño de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena, Santander, en noviembre de 2002. Esta Conferencia ha alcanzado un alto nivel de calidad, como consecuencia de su tradición y madurez, que lo convierte en uno de los acontecimientos más importantes para los circuitos de microelectrónica y la comunidad de diseño de sistemas en el sur de Europa. Desde su origen tiene una gran contribución de Universidades españolas, aunque hoy los autores participan desde catorce países

This book provides the reader with an extensive background in the field of logic-timing simulation and delay modeling. It includes

detailed information on the challenges of logic-timing simulation, applications, advantages and drawbacks. The capabilities of logic-timing are explored using the latest research results that are brought together from previously disseminated materials. An important part of the book is devoted to the description of the ?Degradation Delay Model?, developed by the authors, showing how the inclusion of dynamic effects in the modeling of delays greatly improves the application cases and accuracy of logic-timing simulation. These ideas are supported by simulation results extracted from a wide range of practical applications.Sample Chapter(s)

This book constitutes the refereed proceedings of the 13th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2003, held in Torino, Italy in September 2003. The 43 revised full papers and 18 revised poster papers presented together with three keynote contributions were carefully reviewed and selected from 85 submissions. The papers are organized in topical sections on gate-level modeling and characterization, interconnect modeling and optimization, asynchronous techniques, RTL power modeling and memory optimization, high-level modeling, power-efficient technologies and designs, communication modeling and design, and low-power issues in processors and multimedia.

Digital Timing Macromodeling for VLSI Design Verification first of all provides an extensive history of the development of simulation techniques. It presents detailed discussion of the various techniques implemented in circuit, timing, fast-timing, switch-level timing, switch-level, and gate-level simulation. It also discusses mixed-mode simulation and interconnection analysis methods. The review in Chapter 2 gives an understanding of the advantages and disadvantages of the many techniques applied in modern digital macromodels. The book also presents a wide variety of techniques for performing nonlinear macromodeling of digital MOS subcircuits which address a large number of shortcomings in

existing digital MOS macromodels. Specifically, the techniques address the device model detail, transistor coupling capacitance, effective channel length modulation, series transistor reduction, effective transconductance, input terminal dependence, gate parasitic capacitance, the body effect, the impact of parasitic RC-interconnects, and the effect of transmission gates. The techniques address major sources of errors in existing macromodeling techniques, which must be addressed if macromodeling is to be accepted in commercial CAD tools by chip designers. The techniques presented in Chapters 4-6 can be implemented in other macromodels, and are demonstrated using the macromodel presented in Chapter 3. The new techniques are validated over an extremely wide range of operating conditions: much wider than has been presented for previous macromodels, thus demonstrating the wide range of applicability of these techniques.

The book provides accurate FDTD models for on-chip interconnects, covering most recent advancements in materials and design. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for CNT and GNR based interconnects are presented. Based on the electrical equivalent models the performance comparison among the Cu, CNT and GNR-based interconnects are also discussed in the book. The proposed models are validated with the HSPICE simulations. The book introduces the current research scenario in the modeling of on-chip interconnects. It presents the structure, properties, and characteristics of graphene based on-chip interconnects and the FDTD modeling of Cu based on-chip interconnects. The model considers the non-linear effects of CMOS driver as well as the transmission line effects of interconnect line that includes coupling capacitance and mutual inductance effects. In a more realistic manner, the proposed model includes the effect of width-dependent MFP of the MLGNR while taking into account the edge roughness.

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fint- national workshops. PATMOS 2004 was organized by the University of Patras with technical co-sponsorship from the IEEE Circuits and Systems Society. Over the years, the PATMOS meeting has evolved into an important - ropean event, where industry and academia meet to discuss power and timing aspects in modern integrated circuit and system design. PATMOS provides a forum for researchers to discuss and investigate the emerging challenges in - sign methodologies and tools required to develop the upcoming generations of integrated circuits and systems. We realized this vision this year by providing a technical program that contained state-of-the-art technical contributions, a keynote speech, three invited talks and two embedded tutorials. The technical program focused on timing, performance and power consumption, as well as architectural aspects, with particular emphasis on modelling, design, charac- rization, analysis and optimization in the nanometer era. This year a record 152 contributions were received to be considered for p- sible presentation at PATMOS. Despite the choice for an intense three-day m- ting, only 51 lecture papers and 34 poster papers could be accommodated in the single-track technical program. The Technical Program Committee, with the - sistance of additional expert reviewers, selected the 85 papers to be presented at PATMOS and organized them into 13 technical sessions. As was the case with the PATMOS workshops, the review process was anonymous, full papers were required, and several reviews were received per manuscript.

In DSP Architecture Design Essentials, authors Dejan Marković and Robert W. Brodersen cover a key subject for the successful realization of DSP algorithms for communications, multimedia, and healthcare applications. The book addresses the need for DSP architecture design that maps advanced DSP algorithms to hardware in the most power- and area-efficient way. The key feature of this text is a design methodology based on a high-level design model that leads to hardware implementation with minimum power and area. The methodology includes algorithm-

level considerations such as automated word-length reduction and intrinsic data properties that can be leveraged to reduce hardware complexity. From a high-level data-flow graph model, an architecture exploration methodology based on linear programming is used to create an array of architectural solutions tailored to the underlying hardware technology. The book is supplemented with online material: bibliography, design examples, CAD tutorials and custom software.

Testing and Reliable Design of CMOS Circuits
Integrated Circuit and System Design
A gate-delay model for high-speed CMOS circuits
Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation
Fundamentals
DSP Architecture Design Essentials
A FDTD Approach
DCIS2002
15th International Workshop, PATMOS 2005, Leuven, Belgium, September 21-23, 2005, Proceedings
Advanced Circuits for Emerging Technologies
Logic-timing Simulation and the Degradation Delay Model

The quest for higher performance digital systems for applications such as gen eral purpose computing, signal/image processing, and telecommunications and an increasing cost consciousness have led to a major thrust for high speed VLSI systems implemented in inexpensive and widely available technologies such as CMOS. This monograph, based on the first author's doctoral dissertation, con centrates on the technique of wave pipelining as one method toward achieving this goal. The primary focus of this monograph is to provide a coherent pre

sentation of the theory of wave pipelined operation of digital circuits and to discuss practical design techniques for the realization of wave pipelined circuits in the CMOS technology. Wave pipelining can be applied to a variety of cir cuits for increased performance. For example, many architectures that support systolic computation lend themselves to wave pipelined realization. Also, the wave pipeline design methodology emphasizes the role of controlled clock skew in extracting enhanced performance from circuits that are not deeply pipelined. Wave pipelining (also known as maximal rate pipelining) is a timing method ology used in digital systems to increase the number of effective pipeline stages without increasing the number of physical registers in the pipeline. Using this technique, new data is applied to the inputs of a combinational logic block be fore the outputs due to previous inputs are available thus effectively pipelining the combinational logic and maximizing the utilization of the logic.

These volumes review late 1980s/early 1990s state-of-the-art developments in computer-aided design and analysis techniques. Contributions from researchers and practitioners include discussions of parallel algorithms and fundamental operations in cryptography, systolic arrays and pipelined designs.

Four different CMOS inverter delay models are derived and compared. It is shown that inverter

delay can be estimated with fair accuracy over a wide range of input rise times and loads as the sum of two terms, one proportional to the input rise time, and one proportional to the capacitive load. Methods for estimating device capacitance from HSPICE parameters are presented, as well as means of including added delay due to wire resistance and the use of series transistors. Propagation delay models, for CMOS Digital Circuits, provide an initial design solution for Integrated Circuits. Resources, both monetary and manpower, constrain the design process, leading to the need for a more accurate entry point further along in the design cycle. By verifying an existing propagation delay method, and its resulting delay model, calibration for any given process technology can be achieved. Literature reviews and detailed analysis of each step in the model development allow for greater understanding of each contributing parameter, and ultimately, adjustments to the model calibration result in a more accurate analytical model. An existing model was verified and improved upon using TSMC 0.18um and IBM 0.13um SPICE decks, and the resulting improvements can be used to further assist individuals needing a method and model for deriving an initial circuit design solution for integrated circuits.

The fourth edition of CMOS Digital Integrated Circuits: Analysis and Design continues the well-

established tradition of the earlier editions by offering the most comprehensive coverage of digital CMOS circuit design, as well as addressing state-of-the-art technology issues highlighted by the widespread use of nanometer-scale CMOS technologies. In this latest edition, virtually all chapters have been re-written, the transistor model equations and device parameters have been revised to reflect the sigificant changes that must be taken into account for new technology generations, and the material has been reinforced with up-to-date examples. The broad-ranging coverage of this textbook starts with the fundamentals of CMOS process technology, and continues with MOS transistor models, basic CMOS gates, interconnect effects, dynamic circuits, memory circuits, arithmetic building blocks, clock and I/O circuits, low power design techniques, design for manufacturability and design for testability.

The book will address the-state-of-the-art in integrated circuit design in the context of emerging systems. New exciting opportunities in body area networks, wireless communications, data networking, and optical imaging are discussed. Emerging materials that can take system performance beyond standard CMOS, like Silicon on Insulator (SOI), Silicon Germanium (SiGe), and Indium Phosphide (InP) are explored. Three-dimensional (3-D) CMOS integration and co-integration with sensor technology are described

as well. The book is a must for anyone serious about circuit design for future technologies. The book is written by top notch international experts in industry and academia. The intended audience is practicing engineers with integrated circuit background. The book will be also used as a recommended reading and supplementary material in graduate course curriculum. Intended audience is professionals working in the integrated circuit design field. Their job titles might be : design engineer, product manager, marketing manager, design team leader, etc. The book will be also used by graduate students. Many of the chapter authors are University Professors.

Increasing performance demands in integrated circuits, together with limited energy budgets, force IC designers to find new ways of saving power. One innovative way is the presented adaptive voltage scaling scheme, which tunes the supply voltage according to the present process, voltage and temperature variations as well as aging. The voltage is adapted "on the fly" by means of in-situ delay monitors to exploit unused timing margin, produced by state-of-the-art worst-case designs. This book discusses the design of the enhanced in-situ delay monitors and the implementation of the complete control-loop comprising the monitors, a control-logic and an on-chip voltage regulator. An analytical Markov-based model of the control-loop is derived to

analyze its robustness and stability. Variation-Aware Adaptive Voltage Scaling for Digital CMOS Circuits provides an in-depth assessment of the proposed voltage scaling scheme when applied to an arithmetic and an image processing circuit. This book is written for engineers interested in adaptive techniques for low-power CMOS circuits.

Recent advances in semiconductor technology offer vertical interconnect access (via) that extend through silicon, popularly known as through silicon via (TSV). This book provides a comprehensive review of the theory behind TSVs while covering most recent advancements in materials, models and

designs. Furthermore, depending on the geometry and physical configurations, different electrical equivalent models for Cu, carbon nanotube (CNT) and graphene nanoribbon (GNR) based TSVs are presented. Based on the electrical equivalent models the performance comparison among the Cu, CNT and GNR based TSVs are also discussed.

The International Workshop on Power and Timing Modeling, Optimization, and Simulation PATMOS 2002, was the 12th in a series of international workshops 1 previously held in several places in Europe. PATMOS has over the years evolved into a well-established and outstanding series of open European events on power and timing aspects of integrated circuit design. The increased interest, espe- ally in low-power design, has added further momentum to the interest in this workshop. Despite its growth, the workshop can still be considered as a very - cused conference, featuring high-level scienti?c presentations together with open discussions in a free and easy environment. This year, the workshop has been opened to both regular papers and poster presentations. The increasing number of worldwide high-quality submissions is a measure of the global interest of the international scienti?c

community in the topics covered by PATMOS. The objective of this workshop is to provide a forum to discuss and inves- gate the emerging problems in the design methodologies and CAD-tools for the new generation of IC technologies. A major emphasis of the technical program is on speed and low-power aspects with particular regard to modeling, char- terization, design, and architectures. The technical program of PATMOS 2002 included nine sessions dedicated to most important and current topics on power and timing modeling, optimization, and simulation. The three invited talks try to give a global overview of the issues in low-power and/or high-performance circuit design.

The 11 th IFIP International Conference on Very Large Scale Integration, in Montpellier, France, December 3-5,2001, was a great success. The main focus was about IP Cores, Circuits and System Designs & Applications as well as SOC Design Methods and CAD. This book contains the best papers (39 among 70) that have been presented during the conference. Those papers deal with all aspects of importance for the design of the current and future integrated systems.

System on Chip (SOC) design is today a big challenge for designers, as a SOC may contain

very different blocks, such as microcontrollers, DSPs, memories including embedded DRAM, analog, FPGA, RF front-ends for wireless communications and integrated sensors. The complete design of such chips, in very deep submicron technologies down to 0.13 mm, with several hundreds of millions of transistors, supplied at less than 1 Volt, is a very challenging task if design, verification, debug and industrial test are considered. The microelectronic revolution is fascinating; 55 years ago, in late 1947, the transistor was invented, and everybody knows that it was by William Shockley, John Bardeen and Walter H. Brattein, Bell Telephone Laboratories, which received the Nobel Prize in Physics in 1956. Probably, everybody thinks that it was recognized immediately as a major invention. This book teaches basic and advanced concepts, new methodologies and recent developments in VLSI technology with a focus on low power design. It provides insight on how to use Tanner Spice, Cadence tools, Xilinx tools, VHDL programming and Synopsis to design simple and complex circuits using latest state-of-the art technologies. Emphasis is placed on fundamental transistor circuit-level design concepts.

The objective of this thesis is to devise a delay estimation method that is simple to use when compared to the other delay models while giving accurate results. Our proposed delay estimation method is based on a fundamental delay unit called the 'Unit Delay', derived based on simulation results and analytical calculations. This derived value of Unit delay is constant for a particular technology and is one of the fundamental parameters in the delay estimation. To estimate the delay of a CMOS logic gate, two delay contributing factors, X and K are introduced in this thesis...

High-Performance Digital VLSI Circuit Design is the first book devoted entirely to the design of digital high-performance VLSI circuits. CMOS, BiCMOS and bipolar ciruits are covered in depth, including state-of-the-art circuit structures. Recent advances in both the computer and telecommunications industries demand high-performance VLSI digital circuits. Digital processing of signals demands high-speed circuit techniques for the GHz range. The design of such circuits represents a great challenge; one that is amplified when the power supply is scaled down to 3.3 V. Moreover, the requirements of low-power/high-performance circuits adds an

extra dimension to the design of such circuits. High-Performance Digital VLSI Circuit Design is a self-contained text, introducing the subject of high-performance VLSI circuit design and explaining the speed/power tradeoffs. The first few chapters of the book discuss the necessary background material in the area of device design and device modeling, respectively. High-performance CMOS circuits are then covered, especially the new all-N-logic dynamic circuits. Propagation delay times of high-speed bipolar CML and ECL are developed analytically to give a thorough understanding of various interacting process, device and circuit parameters. High-current phenomena of bipolar devices are also addressed as these devices typically operate at maximum currents for limited device area. Different, new, high-performance BiCMOS circuits are presented and compared to their conventional counterparts. These new circuits find direct applications in the areas of high-speed adders, frequency dividers, sense amplifiers, level-shifters, input/output clock buffers and PLLs. The book concludes with a few system application examples of digital high-performance VLSI circuits. Audience: A vital reference for practicing IC designers. Can be

used as a text for graduate and senior undergraduate students in the area.
In recent years, there has been a great surge of interest in asynchronous circuits, largely through the development of new asynchronous design methodologies. This book provides a comprehensive theory of asynchronous circuits, including modelling, analysis, simulation, specification, verification, and an introduction to their design.

12th International Workshop, PATMOS 2002, Seville, Spain, September 11 - 13, 2002
A Special Issue of Analog Integrated Circuits and Signal Processing, An International Journal Volume 14, Nos. 1/2 (1997)
Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation
Wave Pipelining: Theory and CMOS Implementation
Compact Models and Performance Investigations for Subthreshold Interconnects Differential and Single-ended
Scientific and Technical Aerospace Reports
13th International Workshop, PATMOS 2003, Torino, Italy, September 10-12, 2003, Proceedings
Delay Models for CMOS Circuits
Power and Timing Modeling, Optimization

and Simulation; 14th International Workshop, PATMOS 2004, Santorini, Greece, September 15-17, 2004, Proceedings

Innovative Materials, Modeling and Characterization

This volume features the refereed proceedings of the 17th International Workshop on Power and Timing Modeling, Optimization and Simulation. Papers cover high level design, low power design techniques, low power analog circuits, statistical static timing analysis, power modeling and optimization, low power routing optimization, security and asynchronous design, low power applications, modeling and optimization, and more.

The appropriate interconnect model has changed several times over the past two decades due to the application of aggressive technology scaling. New, more accurate interconnect models are required to manage the changing physical characteristics of integrated circuits. Currently, RC models are used to analyze high resistance nets while capacitive models are used for less resistive interconnect. However, on-chip inductance is becoming more important with integrated circuits operating at higher frequencies, since the inductive impedance is proportional to the frequency. The operating frequencies of integrated circuits have increased dramatically over the past decade and are expected to maintain the same rate of increase over the next decade, approaching 10 GHz by the year 2012. Also, wide wires are frequently encountered in important global nets, such as clock distribution networks and in upper metal layers, and performance requirements are pushing the introduction of new materials for low resistance interconnect, such as copper interconnect already used in many commercial CMOS technologies. On-Chip Inductance in High Speed Integrated Circuits deals with the design and analysis of integrated circuits

with a specific focus on on-chip inductance effects. It has been described throughout this book that inductance can have a tangible effect on current high speed integrated circuits. For example, neglecting inductance and using an RC interconnect model in a production 0.25 mum CMOS technology can cause large errors (over 35%) in estimates of the propagation delay of on-chip interconnect. It has also been shown that including inductance in the repeater insertion design process as compared to using an RC model improves the overall repeater solution in terms of area, power, and delay with average savings of 40.8%, 15.6%, and 6.7%, respectively. On-Chip Inductance in High Speed Integrated Circuits is full of design and analysis techniques for RLC interconnect. These techniques are compared to techniques traditionally used for RC interconnect design to emphasize the effect of inductance. emOn-Chip Inductance in High Speed Integrated Circuits will be of interest to researchers in the area of high frequency interconnect, noise, and high performance integrated circuit design.

In the last few years CMOS technology has become increas ingly dominant for realizing Very Large Scale Integrated (VLSI) circuits. The popularity of this technology is due to its high den sity and low power requirement. The ability to realize very com plex circuits on a single chip has brought about a revolution in the world of electronics and computers. However, the rapid advance ments in this area pose many new problems in the area of testing. Testing has become a very time-consuming process. In order to ease the burden of testing, many schemes for designing the circuit for improved testability have been presented. These design for testability techniques have begun to catch the attention of chip manufacturers. The trend is towards placing increased emphasis on these techniques. Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults. In order to take care of this problem, we need to build fault-tolerant systems. The area of

fault-tolerant computing has steadily gained in importance. Today many universities offer courses in the areas of digital system testing and fault-tolerant computing. Due to the impor tance of CMOS technology, a significant portion of these courses may be devoted to CMOS testing. This book has been written as a reference text for such courses offered at the senior or graduate level. Familiarity with logic design and switching theory is assumed. The book should also prove to be useful to professionals working in the semiconductor industry.

This book provides practical solutions for delay and power reduction for on-chip interconnects and buses. It provides an in depth description of the problem of signal delay and extra power consumption, possible solutions for delay and glitch removal, while considering the power reduction of the total system. Coverage focuses on use of the Schmitt Trigger as an alternative approach to buffer insertion for delay and power reduction in VLSI interconnects. In the last section of the book, various bus coding techniques are discussed to minimize delay and power in address and data buses.

Very Large Scale Integration (VLSI) has become a necessity rather than a specialization for electrical and computer engineers. This unique text provides Engineering and Computer Science students with a comprehensive study of the subject, covering VLSI from basic design techniques to working principles of physical design automation tools to leading edge application-specific array processors. Beginning with CMOS design, the author describes VLSI design from the viewpoint of a digital circuit engineer. He develops physical pictures for CMOS circuits and demonstrates the top-down design methodology using two design projects - a microprocessor and a field programmable gate array. The author then discusses VLSI testing and dedicates an entire chapter to the working principles, strengths, and weaknesses of ubiquitous physical design tools. Finally, he unveils the frontiers of VLSI. He

emphasizes its use as a tool to develop innovative algorithms and architecture to solve previously intractable problems. VLSI Design answers not only the question of "what is VLSI," but also shows how to use VLSI. It provides graduate and upper level undergraduate students with a complete and congregated view of VLSI engineering.

The book provides a detailed analysis of issues related to sub-threshold interconnect performance from the perspective of analytical approach and design techniques. Particular emphasis is laid on the performance analysis of coupling noise and variability issues in sub-threshold domain to develop efficient compact models. The proposed analytical approach gives physical insight of the parameters affecting the transient behavior of coupled interconnects. Remedial design techniques are also suggested to mitigate the effect of coupling noise. The effects of wire width, spacing between the wires, wire length are thoroughly investigated. In addition, the effect of parameters like driver strength on peak coupling noise has also been analyzed. Process, voltage and temperature variations are prominent factors affecting sub-threshold design and have also been investigated. The process variability analysis has been carried out using parametric analysis, process corner analysis and Monte Carlo technique. The book also provides a qualitative summary of the work reported in the literature by various researchers in the design of digital sub-threshold circuits. This book should be of interest for researchers and graduate students with deeper insights into sub-threshold interconnect models in particular. In this sense, this book will best fit as a text book and/or a reference book for students who are initiated in the area of research and advanced courses in nanotechnology, interconnect design and modeling.

SOC Design Methodologies

Techniques

Analog Design Issues in Digital VLSI Circuits and Systems

10th International Workshop, PATMOS 2000, Göttingen, Germany, September 13-15, 2000 Proceedings
High-Performance Digital VLSI Circuit Design
Low-Power CMOS Circuits
Delay Estimation in CMOS Circuits
Nanoscale CMOS
Asynchronous Circuits
A Comprehensive Delay Model for CMOS CML Circuits
Materials, Models, Design, and Performance