Circuits And Algorithms

This book covers algorithmic and hardware implementation techniques to enable embedded deep learning. The

authors describe synergetic design approaches on the application-, algorithmic-, computer architecture-, and circuit-level that will help in achieving the goal of reducing the computational cost of deep learning

algorithms. The impact of these techniques is displayed in four silicon prototypes for embedded deep learning. Gives a wide overview of a series of effective solutions for energy-efficient neural

networks on battery constrained wearable devices; Discusses the optimization of neural networks for embedded deployment on all levels of the design hierarchy – applications, algorithms,

hardware architectures, and circuits - supported by real silicon prototypes; Elaborates on how to design efficient Convolutional Neural Network processors, exploiting parallelism and data-reuse, sparse

operations, and low-precision computations; Supports the introduced theory and design concepts by four real silicon prototypes. The physical realization's implementation and achieved performances

are discussed elaborately to illustrated and highlight the introduced cross-layer design concepts.
This book is based on a collection of the past exams for the VLSI Analog Signal Processing Circuits class

(EEE598) the author offered in the School of Engineering at Arizona State University. The topics cover various aspects of the design, analysis and application of VLSI analog signal processing circuits. This

book is intended to be used together with the VLSI Analog Signal Processing Circuits textbook by the same author. It can also be used alone for the experienced readers.

The last decade has brought

explosive growth in the technology for manufac turing integrated circuits. Integrated circuits with several hundred thousand transistors are now commonplace. This manufacturing capability,

combined with the economic benefits of large electronic systems, is forcing a revolution in the design of these systems and providing a challenge to those people in terested in integrated system design. Modern

circuits are too complex for an individual to comprehend completely. Managing tremendous complexity and automating the design process have become crucial issues. Two groups are interested in dealing with

complexity and in developing algorithms to automate the design process. One group is composed of practi tioners in computer-aided design (CAD) who develop computer programs to aid the circuit-design process. The second

group is made up of computer scientists and mathemati'::~l\ns who are interested in the design and analysis of efficient combinatorial aJ::,orithms. These two groups have developed separate bodies of

literature and, until recently, have had relatively little interaction. An obstacle to bringing these two groups together is the lack of books that discuss issues of importance to both groups in

the same context. There are many instances when a familiarity with the literature of the other group would be beneficial. Some practitioners could use known theoretical results to improve their "cut and try"

heuristics. In other cases, theoreticians have published impractical or highly abstracted toy formulations, thinking that the latter are important for circuit layout.

This book contains extended

and revised versions of the best papers presented at the 20th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2012, held in Santa Cruz, CA, USA, in October 2012. The 12

papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the

current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these

systems.
Arithmetic Circuits: A Survey of Recent Results and Open Questions surveys the field of arithmetic circuit complexity. The focus is mainly on the most interesting and accessible

research directions. It covers the main results and techniques, with an emphasis on works from the last two decades

This book presents an excellent collection of contributions addressing

different aspects of high-level synthesis from both industry and academia. It includes an overview of available EDA tool solutions and their applicability to design problems.

Algorithms and Data

Structures in VLSI Design

Algorithms for Retiming Level-clocked Circuits and Their Use in Increasing Circuit Robustness

DSP Integrated Circuits

Algorithms for VLSI Physical Design Automation

VLSI Analog Circuits: Algorithms, Architecture, Modeling, and Circuit Implementation

Algorithms for Routing of VLSI Circuits

Novel Algorithms for Fast Statistical Analysis of

Scaled Circuits

Algorithms and Circuits

Exact Exponential Algorithms

Quantum Algorithms Via Linear Algebra

On Algorithms for Finding All Circuits of a Graph

We improve the size bound for

parallel circuits and algorithms for the division problem. Keywords include: Division, Boolean circuits, PRAM algorithms for the division problem. In modern photovoltaic systems, there is an ever-increasing need to improve the system efficiency, to

detect internal faults and to guarantee service continuity. The only way to meet these objectives is to utilize and create synergies between diagnostic techniques and control algorithms. Diagnostic methods can be implemented through module-

dedicated electronics, by running on real-time embedded systems or by using a huge database on the cloud, profiting from artificial intelligence, machine learning, and classifiers. Model-based diagnostic approaches and data-driven methods are

attracting the interest of the scientific community for the automatic detection of phenomena like the occurrence of hot spots, the increase of the ohmic losses, the degradation due to unexpected potentials (PID), switch failures in power electronic

converters, and also the reduction of the power production due to soiling or partial shadowing. The detection of malfunctioning or even faults affecting the whole power conversion chain, from the photovoltaic modules to the power conversion stages, allows to

perform proper control actions, also in terms of MPPT. Control algorithms, running on an embedded system, are optimized, e.g., through the online adaptation of their own parameters, by suitably processing data coming from the diagnostic

algorithms. This book presents recent and original results about the diagnostic approaches to photovoltaic modules and related power electronics and control strategies with the aim to maximize the photovoltaic output power, to increase the whole

system efficiency and to guarantee service continuity.
DSP Integrated Circuits establishes the essential interface between theory of digital signal processing algorithms and their implementation in full-custom CMOS technology. With an

emphasis on techniques for co-design of DSP algorithms and hardware in order to achieve high performance in terms of throughput, low power consumption, and design effort, this book provides the professional engineer, researcher, and student with

a firm foundation in the theoretical as well as the practical aspects of designing high performance DSP integrated circuits. Centered around three design case studies, DSP Integrated Circuits thoroughly details a high-performance FFT processor, a

2-D Discrete Cosine Transform for HDTV, and a wave digital filter for interpolation of the sampling frequency. The case studies cover the essential parts of the design process in a top-down manner, from specification of algorithm design and

optimization, scheduling of operations, synthesis of optimal architectures, realization of processing elements, to the floor-planning of the integrated circuit. Details the theory and design of digital filters - particularly wave digital filters, multi-

rate digital filters, fast Fourier transforms (FFT's), and discrete cosine transforms (DCT's) Follows three complete "real-world" case studies throughout the book Provides complete coverage of finite word length effects in DSP algorithms In-

depth survey of the computational properties of DSP algorithms and their mapping to optimal architectures Outlines DSP architectures and parallel, bit-serial, and distributed arithmetic Presents the design process in a top-down

manner and incorporates numerous problems and solutions
A comprehensive guide to the fundamental concepts, designs, and implementation schemes, performance considerations, and applications of arithmetic circuits for

DSP Arithmetic Circuits for DSP Applications is a complete resource on arithmetic circuits for digital signal processing (DSP). It covers the key concepts, designs and developments of different types of arithmetic circuits, which can be used for

improving the efficiency of implementation of a multitude of DSP applications. Each chapter includes various applications of the respective class of arithmetic circuits along with information on the future scope of research. Written for students,

engineers, and researchers in electrical and computer engineering, this comprehensive text offers a clear understanding of different types of arithmetic circuits used for digital signal processing applications. The text includes contributions from

noted researchers on a wide range of topics, including a review of circuits used in implementing basic operations like additions and multiplications; distributed arithmetic as a technique for the multiplier-less implementation of inner products for

DSP applications; discussions on look up table-based techniques and their key applications; CORDIC circuits for calculation of trigonometric, hyperbolic and logarithmic functions; real and complex multiplications, division, and square-root; solution of

linear systems; eigenvalue estimation; singular value decomposition; QR factorization and many other functions through the use of simple shift-add operations; and much more. This book serves as a comprehensive resource, which describes the

arithmetic circuits as fundamental building blocks for state-of-the-art DSP and reviews in - depth the scope of their applications.

ABSTRACT: The occurrence of transient faults like soft errors in computer circuits poses a significant

challenge to the reliability of computer systems. Soft error, which occurs when the energetic neutrons coming from space or the alpha particles arising out of packaging materials hit the transistors, may manifest themselves as a bit flip in the

memory element or as a transient glitch generated at any internal node of combinational logic, which may subsequently propagate to and be captured in a latch. Although the problem of soft errors was earlier only a concern for space applications,

aggressive technology scaling trends have exacerbated the problem to modern VLSI systems even for terrestrial applications. In this dissertation, we explore techniques at all levels of the design flow to reduce the vulnerability of VLSI systems

against soft errors without compromising on other design metrics like delay, area and power. We propose new models for estimating soft errors for storage structures and combinational logic. While soft errors in caches are

estimated using the vulnerability metric, soft errors in logic circuits are estimated using two new metrics called the glitch enabling probability (GEP) and the cumulative probability of observability (CPO). These metrics, based on signal probabilities

of nets, accurately model soft errors in radiation-aware synthesis algorithms and helps in efficient exploration of the design solution space during optimization. At the physical design level, we leverage the use of larger netlengths to provide larger RC

ladders for effectively filtering out the transient glitches. Towards this, a new heuristic has been developed to selectively assign larger wirelengths to certain critical nets. This reduces the delay and area overhead while improving the immunity to soft

errors. Based on this, we propose two placement algorithms based on simulated annealing and quadratic programming which significantly reduce the soft error rates of circuits. At the circuit level, we develop techniques for hardening circuit

nodes using a novel radiation jammer technique. The proposed technique is based on the principles of a RC differentiator and is used to isolate the driven cell from the driving cell which is being hit by a radiation strike. Since the blind insertion of radiation

blocker cells on all circuit nodes is expensive, candidate nodes are selected for insertion of these cells using a new metric called the probability of radiation blocker circuit insertion (PRI). We investigate a gate sizing algorithm, at the logic level, in

which we simultaneously optimize both the soft error rate (SER) and the crosstalk noise besides the power and performance of circuits while considering the effect of process variations. The reliability centric gate sizing technique has been formulated

as a mathematical program and is efficiently solved. At the architectural level, we develop solutions for the correction of multi-bit errors in large L2 caches by controlling or mining the redundancy in the memory hierarchy and methods to increase the

amount of redundancy in the memory hierarchy by employing a redundancy-based replacement policy, in which the amount of redundancy is controlled using a user defined redundancy threshold. The novel architectures and the new

reliability-centric synthesis algorithms proposed for the various design abstraction levels have been shown to achieve significant reduction of soft error rates in current nanometer circuits. The design techniques, algorithms and architectures can be

integrated into existing design flows. A VLSI system implementation can leverage on the architectural solutions for the reliability of the caches while the custom hardware synthesized for the VLSI system can be protected against radiation strikes by utilizing

the circuit level, logic level and layout level optimization algorithms that have been developed.
First-ever comprehensive introduction to the major new subject of quantum computing and quantum information.

A Survey of Recent Results and Open Questions
Partitioning, Placement, and Routing
Algorithms for High Compelexity Integrated Circuits
Foundations of Digital Signal Processing

Methods, Algorithms and Circuits for Photovoltaic Systems Diagnosis and Control

Dynamic Programming Multi-Objective Combinatorial Optimization

Algorithms for Performance Driven

Design of Integrated Circuits High-Level Synthesis 20th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2012, Santa Cruz, CA, USA, October 7-10, 2012, Revised Selected Papers

VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design
Circuits and Algorithms
Complex Binary Number System

This textbook teaches in one, coherent presentation the three distinct topics of analysis of electronic circuits,

mathematical numerical algorithms and coding in a software such as MATLAB®. By combining the capabilities of circuit simulators and mathematical software, the author teaches key concepts of circuit analysis and algorithms, using a modern approach. The DC, Transient,

AC, Noise and behavioral analyses are implemented in MATLAB to study the complete characteristics of a variety of electronic circuits, such as amplifiers, rectifiers, hysteresis circuits, harmonic traps and passes, polyphaser filters, directional couplers, electro-static discharge and

piezoelectric crystals. This book teaches basic and advanced circuit analysis, by incorporating algorithms and simulations that teach readers how to develop their own simulators and fully characterize and design electronic circuits. Teaches students and practitioners DC, AC, Transient,

Noise and Behavioral analyses using MATLAB; Shows readers how to create their own complete simulator in MATLAB by adding materials learned in all 6 chapters of the book; Balances theory, math and analysis; Introduces many examples such as noise minimization, parameter

optimization, power splitters, harmonic traps and passes, directional couplers, polyphase filters and electro-static discharge that are hardly referenced in other textbooks; Teaches how to create the fundamental analysis functions such as linear and nonlinear equation

solvers, determinant calculation, random number generation and Fast Fourier transformation rather than using the built-in native MATLAB codes.

Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD

professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are

discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the

background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding advanced

material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design.
From the explosion of interest, research, and applications of evolutionary computation a new field

emerges-evolutionary electronics. Focused on applying evolutionary computation concepts and techniques to the domain of electronics, many researchers now see it as holding the greatest potential for overcoming the drawbacks of conventional design techniques. Evolutionary Electronics:

Automatic Design of Electronic Circuits and Systems by Genetic Algorithms formally introduces and defines this area of research, presents its main challenges in electronic design, and explores emerging technologies. It describes the evolutionary computation paradigm

and its primary algorithms, and explores topics of current interest, such as multi-objective optimization. The authors examine numerous evolutionary electronics applications, draw conclusions about those applications, and sketch the future of evolutionary computation and its

applications in electronics. In coming years, the appearance of more and more advanced technologies will increase the complexity of optimization and synthesis problems, and evolutionary electronics will almost certainly become a key to solving those problems. Evolutionary

Electronics is your key to discovering and unlocking the potential of this promising new field.
One of the most notable features of nanometer scale CMOS technology is the increasing magnitude of variability of the key device parameters affecting performance of

integrated circuits. The growth of variability can be attributed to multiple factors, including the difficulty of manufacturing control, the emergence of new systematic variation-generating mechanisms, and most importantly, the increase in atomic-scale randomness, where

device operation must be described as a stochastic process. In addition to wide-sense stationary stochastic device variability and temperature variation, existence of non-stationary stochastic electrical noise associated with fundamental processes in integrated-circuit devices represents

an elementary limit on the performance of electronic circuits. In an attempt to address these issues, Stochastic Process Variation in Deep-Submicron CMOS: Circuits and Algorithms offers unique combination of mathematical treatment of random process variation, electrical noise and

temperature and necessary circuit realizations for on-chip monitoring and performance calibration. The associated problems are addressed at various abstraction levels, i.e. circuit level, architecture level and system level. It therefore provides a broad view on the various solutions that

have to be used and their possible combination in very effective complementary techniques for both analog/mixed-signal and digital circuits. The feasibility of the described algorithms and built-in circuitry has been verified by measurements from the silicon

prototypes fabricated in standard 90 nm and 65 nm CMOS technology. An excellent introductory text, this book covers the basic theoretical, algorithmic and real-time aspects of digital signal processing (DSP). Detailed information is provided on off-line, real-time and DSP

programming and the reader is effortlessly guided through advanced topics such as DSP hardware design, FIR and IIR filter design and difference equation manipulation. Abstract: "This report explores the use of circuits as practical models for the semantics of parallel algorithms. It is

shown that circuits are useful for explaining the meaning of parallel algorithms, just as a textual notation is useful for comprehending the algorithms underlying circuits. The relationship between circuits and algorithms is developed to the depth where it becomes clear that they are

equivalent in expressibility. In order to express algorithms that involve re-use of resources, the concept of the data barrier is introduced and used to extend the algorithm-circuit relationship to cover pipelined and systolic circuits, in particular."

Efficient Parallel Circuits and

Algorithms for Division
Circuit Simulation Methods and Algorithms
Efficient Algorithms for Area Minimization in Floorplanning of VLSI Circuits
With Case Studies
Embedded Deep Learning

Architectures and Algorithms for Mitigation of Soft Errors in Nanoscale VLSI Circuits
Quantum Circuits and Quantum Algorithms
Arithmetic Circuits for DSP Applications
Theory, Algorithms and Hardware

Design
A Primer
VLSI Analog Signal Processing
Circuits

Circuit Simulation Methods and Algorithms provides a step-by-step theoretical

consideration of methods, techniques, and algorithms in an easy-to-understand format. Many illustrations explain more difficult problems and present instructive circuits. The

book works on three levels: The simulator-user level for practitioners and students who want to better understand circuit simulators. The basic theoretical level, with

examples, dedicated to students and beginning researchers. The thorough level for deep insight into circuit simulation based on computer experiments using PSPICE

and OPTIMA. Only basic mathematical knowledge, such as matrix algebra, derivatives, and integrals, is presumed. The story of how Indians, Spaniards, Frenchmen,

Mexicans, and Americans have made New Mexico the growing and productive state it is today
As VLSI technology moves to the nanometer scale for transistor feature sizes,

the impact of manufacturing imperfections result in large variations in the circuit performance. Traditional CAD tools are not well-equipped to

handle this scenario, since they do not model this statistical nature of the circuit parameters and performances, or if they do, the existing techniques tend to be over-

simplified or intractably slow. Novel Algorithms for Fast Statistical Analysis of Scaled Circuits draws upon ideas for attacking parallel problems in other technical fields, such as

computational finance, machine learning and actuarial risk, and synthesizes them with innovative attacks for the problem domain of integrated circuits. The

result is a set of novel solutions to problems of efficient statistical analysis of circuits in the nanometer regime. Since the second half of the 1980s asynchronous

circuits have been the subject of a great deal of research following a period of relative oblivion. The lack of interest in asynchronous techniques was motivated

by the progressive shift towards synchronous design techniques that had much more structure and were much easier to verify and synthesize. System design requirements made it

impossible to eliminate totally the use of asynchronous circuits. Given the objective difficulty encountered by designers, the asynchronous components of

electronic systems such as interfaces became a serious bottleneck in the design process. The use of new models and some theoretical breakthroughs made it possible to

develop asynchronous design techniques that were reliable and effective. This book describes a variety of mathematical models and of algorithms that form the

backbone and the body of a new design methodology for asyn chronous design. The book is intended for asynchronous hardware designers, for computer-aided tool experts, and

for digital designers interested in ex ploring the possibility of designing asynchronous circuits. It requires a solid mathematical background in discrete

event systems and algorithms. While the book has not been written as a textbook, nevertheless it could be used as a reference book in an advanced course in logic

synthesis or asynchronous design.
One of the main problems in chip design is the enormous number of possible combinations of individual chip elements

within a system, and the problem of their compatibility. The recent application of data structures, efficient algorithms, and ordered binary decision diagrams

(OBDDs) has proven vital in designing the computer chips of tomorrow. This book provides an introduction to the foundations of this interdisciplinary research

area, emphasizing its applications in computer aided circuit design. For a long time computer scientists have distinguished between fast and slow algo rithms. Fast

(or good) algorithms are the algorithms that run in polynomial time, which means that the number of steps required for the algorithm to solve a problem is bounded by some

polynomial in the length of the input. All other algorithms are slow (or bad). The running time of slow algorithms is usually exponential. This book is about bad algorithms.

There are several reasons why we are interested in exponential time algorithms. Most of us believe that there are many natural problems which cannot be solved by

polynomial time algorithms. The most famous and oldest family of hard problems is the family of NP complete problems. Most likely there are no polynomial

time al gorithms solving these hard problems and in the worst case scenario the exponential running time is unavoidable. Every combinatorial problem is solvable in ?nite time by

enumerating all possi ble solutions, i. e. by brute force search. But is brute force search always unavoid able? De?nitely not. Already in the nineteen sixties and

seventies it was known that some NP complete problems can be solved signi?cantly faster than by brute force search. Three classic examples are the following algorithms

for the TRAVELLING SALESMAN problem, MAXIMUM INDEPENDENT SET, and COLORING.

Algorithms and Computational Techniques

Computer-aided Analysis of

Electronic Circuits

Algorithms for Synthesis and Testing of Asynchronous Circuits

Computational Electronic Circuits

On the Study of Efficient

Timing Analysis Algorithms for VLSI Circuits

Stochastic Process Variation in Deep-Submicron CMOS

Algorithms for Synthesis and Verification of Timed

Circuits and Systems

from Algorithm to Digital Circuit

Quantum Computation and Quantum Information

Evolutionary Electronics

Automatic Design of

Electronic Circuits and Systems by Genetic Algorithms

Methodology for the Digital Calibration of Analog Circuits and Systems shows how to relax the extreme design constraints in analog

circuits, allowing the realization of high-precision systems even with low-performance components. A complete methodology is proposed, and three applications are detailed. To start with, an in-depth analysis of existing compensation techniques for analog

circuit imperfections is carried out. The M/2+M sub-binary digital-to-analog converter is thoroughly studied, and the use of this very low-area circuit in conjunction with a successive approximations algorithm for digital compensation is described. A complete

methodology based on this compensation circuit and algorithm is then proposed. The detection and correction of analog circuit imperfections is studied, and a simulation tool allowing the transparent simulation of analog

circuits with automatic compensation blocks is introduced. The first application shows how the sub-binary M/2+M structure can be employed as a conventional digital-to-analog converter if two calibration and radix conversion algorithms are

implemented. The second application, a SOI 1T DRAM, is then presented. A digital algorithm chooses a suitable reference value that compensates several circuit imperfections together, from the sense amplifier offset to the dispersion of the memory read

currents. The third application is the calibration of the sensitivity of a current measurement microsystem based on a Hall magnetic field sensor. Using a variant of the chopper modulation, the spinning current technique, combined with a second

modulation of a reference signal, the sensitivity of the complete system is continuously measured without interrupting normal operation. A thermal drift lower than 50 ppm/°C is achieved, which is 6 to 10 times less than in state-of-the-art

implementations. Furthermore, the calibration technique also compensates drifts due to mechanical stresses and ageing.

Quantum computing explained in terms of elementary linear algebra, emphasizing computation and

algorithms and requiring no background in physics.
VLSI Signal Processing Principles, Practices, and Applications This comprehensive resource shows how very-large-scale integration (VLSI) technology can be effectively deployed

in real-world electronics to meet cost, power, function, and reliability requirements. VLSI Analog Circuits: Algorithm, Architecture, Modeling, and Circuit Implementation, Second Edition, is a textbook for advanced electrical engineering courses that

shows, step-by-step, how to analyze and solve practical design problems using VLSI. You will get up-to-date discussions on VLSI passive, active-RC, MOS-C, Gm-C, CTI, SC, and SI analog filter circuits. Mixed-mode configurations, VLSI RF signal

processing, and circuit tuning techniques are explained in full detail. Coverage includes: • VLSI continuous-time signal processing fundamentals • VLSI active-RC, MOS-C, and VLSI Gm-C circuits • VLSI continuous-time current-mode filters • VLSI discrete-

time signal processing systems • VLSI switched-capacitor and switched-current circuits • Frequency-scaling and transformation techniques • Mixed-mode VLSI analog signal processing • Component and ladder simulation-based VLSI design •

Practical design aspects of VLSI analog filters • VLSI RF signal processing circuits • Digital-based analog signal processing circuits This book is a compilation of the entire research work on the topic of Complex Binary Number System

(CBNS) carried out by the author as the principal investigator and members of his research groups at various universities during the years 2000-2012. Pursuant to these efforts spanning several years, the realization of CBNS as a viable alternative to

represent complex numbers in an "all-in-one" binary number format has become possible and efforts are underway to build computer hardware based on this unique number system. It is hoped that this work will be of interest to anyone involved in computer

arithmetic and digital logic design and kindle renewed enthusiasm among the engineers working in the areas of digital signal and image processing for developing newer and efficient algorithms and techniques incorporating CBNS.

The Circuit Model for Parallel Algorithms

OBDD - Foundations and Applications

Methodology for the Digital Calibration of Analog Circuits and Systems

Algorithms, Architectures and Circuits

for Always-on Neural Network Processing

Arithmetic Circuits

Combinatorial Algorithms for Integrated Circuit Layout

Simulation and Analysis with MATLAB®

Algorithms for the Electrical Optimization of Digital MOS Circuits